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EXAMINER	
KHOO, FOONG LIN	
ART UNIT	**PAPER NUMBER**
2664	

DATE MAILED: 12/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/024,553	RAHIM, RAMI	
	Examiner	Art Unit	
	F. Lin Khoo	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-14 and 16-26* is/are rejected.

7)☒ Claim(s) *8 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: On page 15, paragraph [0051], line 2, the reorder engine is identified as 522. However, in Fig. 3, the reorder engine is identified as 322.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1- 5, 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Rana et al. (U.S. Patent No. 6,781,992).

Regarding Claim 1, Rana et al. discloses a queue engine (reordering device) comprising: a reorder buffer configured to store information relating to data items, each of the data items being associated a sequence number chosen from a sequence number space, the sequence number indicating a relative order of the data items (Fig. 1, element 26 (PDU assembler) and element 34 (IP reordering unit) together forms a

reorder buffer. See col 2, lines 42-53, col 5, lines 9-21); a reorder buffer pointer configured to store a value indicating a rearmost active entry of the reorder buffer relative to the sequence number space (Fig. 1, element 24 (link list memory) is equivalent to a reorder buffer pointer. The link lists in link list memory 24 are used by queue engine 10 to track pointers associated with data packets stored in packet memory 20. A next field for storing the pointer to the next associated block or PDU is associated with rearmost active entry of the reorder buffer. See col 3, lines 47-49. Fig. 3C, col 6, line 66- col 7, line 10. Also see Fig. 3E and 3G, the tail_ptr to PDU linked list is also associated with rearmost active entry of the reorder buffer); and a reorder engine configured to receive the data items, the reorder engine classifying each of the received data items based on the sequence number of the data item and the value of the reorder buffer pointer, the reorder engine determining whether to store the information relating to the received data items in the reorder buffer based on the classification (Fig. 1, element 44 (IRU memory) is associated with a reorder engine. IP reordering unit 34 uses IRU memory 44 to keep track of windows which reflect PDUs belonging to a particular traffic flow and where each PDU belongs in sequence. Keeping track of windows belonging to a particular traffic flow is associated with the reorder engine classifying each of the received data items based on the sequence number of the data item and the value of the reorder buffer pointer, the reorder engine determining whether to store the information relating to the received data items in the reorder buffer based on the classification. See col 5, lines 22-24).

Regarding Claim 2, Rana et al. discloses: an interface configured to receive the data items from a network and to transmit information identifying the data items to the reorder engine (Fig. 1. element 12 (input) and element 14 (input interface) is associated with an interface configured to receive the data items from a network and to transmit information identifying the data items to the reorder engine. See col 3, lines 23-42).

Regarding Claim 3, Rana et al. discloses: an external memory configured to receive the data items from the interface and to store the data items (Fig. 1, element 20 (packet memory). See col 3, lines 29-33).

Regarding Claim 4, Rana et al. discloses wherein the reorder buffer includes, for each entry in the reorder buffer: a first storage portion for storing an address of the data item stored in the external memory (Fig. 3D and 3F show the window index which is associated with the address of the data item stored in the external memory. See col 7, lines 50-55), and a second storage portion for storing information indicating whether the address stored in the first portion is valid (Fig. 3D through 3G show the valid bit. See col 7, lines 31-34, lines 50-55).

Regarding Claim 5, Rana et al. discloses wherein the reorder buffer additionally includes, for each entry in the reorder buffer: a third storage portion for storing information indicating a type of the data item (Fig. 3D show first_frag

and last_frag which are associated with a type of the data item. See col 7, lines 31-34).

Regarding Claim 12, Rana et al. discloses a method of ordering data items comprising: receiving the data items, the received data items being associated with a sequence number chosen from a sequence number space, the sequence number indicating a relative order of the data items (Fig. 1, col 2, lines 42-53, col 5, lines 9-21); classifying the received data items as one of a plurality of possible classifications based on the sequence number of the data items and a value that defines a position of a reorder buffer in the sequence number space (Fig. 1; col 5, lines 22-24); and processing the data items based on the classifications (col 5, lines 14-30).

4. Claims 18 - 24, 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Westbrook et al. (U.S. Patent No. 6,832,261).

Regarding Claim 18, Westbrook et al. discloses a network device comprising: a data transmission component (Fig 2A, element 200 (distributor(s)), col 7, lines 39-48); and a plurality of processing elements connected by the data transmission component, the processing elements communicating with one another by transmitting data items over the data transmission component (Fig. 2A, elements 203A, 203B....203N (distributed resequencing and/or reassembly

components are associated with a plurality of processing elements connected by the data transmission component); col 7, lines 39-64), the processing elements each including a reorder component configured to arrange received data items into an order corresponding to an order in which the data items were transmitted, each of the reorder components (Fig. 2A, elements 203A, 203B....203N, each include a resequencing component equivalent to a reorder component. See col 7, lines 12-18) including:

a reorder buffer configured to store the data items, each of the data items including a sequence number chosen from a sequence number space, the sequence number indicating the order of the data items (Fig. 2C, Fig. 4A, element 402, Fig 5, col 8, line 61 through col 9, line 23; col 12, lines 38-62. Packet resequencer is associated with a reorder buffer), and

a reorder engine configured to classify the data items based on the sequence number of the data items and based on a position of the reorder buffer relative to the sequence number space, the reorder engine determining whether to store the data items in the reorder buffer based on the classification of the data items (Fig 4A, element 415 and Fig. 8; col 13, line 53 through col 14, line 12. The queue manager is associated with the reorder engine. The reassembled packet is stored in queue memory 806 based on its destination, priority and/or class of service).

Regarding Claim 19, Westbrook et al. discloses a reorder buffer pointer that stores a value indicating the position of the reorder buffer relative to the sequence number space (Fig. 4C, element 449; Fig. 7 (packet memory manager is associated with a reorder buffer pointer where the payload pointer points to the corresponding packet payload 449 stored in the packet memory manager 420). See col 11, line 66 through col 12, line 18 and col 14, lines 56-63).

Regarding Claim 20, Westbrook et al. discloses wherein the network device is a router (Fig. 1A, elements 100 and 102; col 2, lines 54-60, col 5, lines 28-67).

Regarding Claim 21, Westbrook et al. discloses wherein the reorder buffer includes, for each entry in the reorder buffer: a first storage portion for storing information indicating whether the address stored in the first portion is valid (Fig. 6, col 14, lines 13-34. A packet descriptor consist of a packet header that contains addresses. If the packet header received is not the first sub-packet of a packet and there is no valid packet descriptor allocated for this packet, reassembly manager 604 waits until it receives a packet descriptor from ring update controller 602, which receives the valid packet descriptor from one of the other reassembly managers 604 in the system. The validity obtained from the packet descriptor is associated with storing information indicating whether the address stored in the first portion is valid).

Regarding Claim 22, Westbrook et al. discloses wherein the reorder buffer additionally includes, for each entry in the reorder buffer: a second storage portion for storing information indicating a type of the data item (Fig. 4B, element 431A includes a packet type. See col 11, lines 21-35).

Regarding Claim 23, Westbrook et al. discloses wherein the classification utilizes a plurality of regions, including: a first region corresponding to the sequence number of the data item falling within a sequence number range covered by the reorder buffer (Fig. 4C, element 443A is a first region corresponding to the sequence number of the data item falling within a sequence number range covered by the reorder buffer. See col 11, line 66 through col 12, line18), and a second region corresponding to the sequence number of the data item falling within a sequence number range extending from the value stored in the reorder buffer pointer to a predetermined range beyond the value stored in the reorder buffer pointer (Fig 4C, element 443B is the second region. See col 11, line 66 through col 12, line18).

Regarding Claim 24, Westbrook et al. discloses wherein the plurality of regions further includes: a third region corresponding to the sequence number of the data item falling within a sequence number range outside of the first and

second regions (Fig 4C, element 443C is the third region. See col 11, line 66 through col 12, line18).

Regarding Claim 26, Westbrook et al. discloses a system for ordering data items, comprising: means for receiving the data items, the received data items being associated with a sequence number chosen from a sequence number space, the sequence numbers indicating a relative order of the data items (Fig. 2C, Fig. 4A, element 402, Fig 5, col 8, line 61 through col 9, line 23; col 12, lines 38-62); means for classifying the received data items into one of a plurality of possible classifications based on the sequence number of the data items in relation to a value that defines the position of a reorder buffer in the sequence number space (Fig 4A, element 415 and Fig. 8; col 13, line 53 through col 14, line 12. The reassembled packet is stored in queue memory 806 based on its destination, priority and/or class of service. The destination, priority and/or class of service is one of a plurality of possible classifications based on the sequence number of the data items); and means for processing the data items in the reorder buffer based on the classifications of the data items (Fig 4A, element 415 and Fig. 8; col 13, line 53 through col 14, line 12. The reassembled packet is stored in queue memory 806 based on its destination, priority and/or class of service and this is associated with the classifications of the data items. At the appropriate time, as determined by control logic 808, the queue manager extracts from one of its queues a data structure describing the corresponding

reassembled packet to be sent from the distributed resequencing and reassembly component 303B, and places it in outgoing buffer 804 which is associated with processing the data items in the reorder buffer based on the classifications of the data items).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6, 7, 9, 10, 11, 13, 14, 16, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rana et al. (U.S. Patent No. 6,781,992) in view of Kyker et al. (U.S. Patent No. 6,026,477).

Regarding Claim 6, Rana et al. discloses a queue engine for reassembling and reordering data packets in a network. Rana et al. does not disclose wherein the classifying utilizes a plurality of regions including: a first region corresponding to the sequence number of the data item falling within a sequence number range covered by the reorder buffer, and a second region corresponding to the sequence number of the data item falling within a sequence number range extending from a head of the reorder

buffer to a predetermined range beyond the head of the reorder buffer. Kyker et al. discloses a first region corresponding to the sequence number of the data item falling within a sequence number range covered by the reorder buffer (Fig. 1, Fig. 3, element 30 (in-order front end) is associated with the first region. See col 2, line 33 through col 3, line 21) and a second region corresponding to the sequence number of the data item falling within a sequence number range extending from a head of the reorder buffer to a predetermined range beyond the head of the reorder buffer (Fig. 1, Fig. 3, element 32 (out of order middle) is associated with the second region. See col 2, line 33 through col 3, line 21). At the time the invention was made it would have been obvious to a person of ordinary skill in the art to modify the system of Rana et al. by using the features as taught by Kyker et al. for a more efficient technique to recover from a mispredicted branch in order to reduce the front end stall time (see col 3, lines 43-45).

Regarding Claim 7, Rana et al. discloses a queue engine for reassembling and reordering data packets in a network. Rana et al. does not disclose wherein the plurality of regions further includes: a third region corresponding to the sequence number of the data item falling within a sequence number range outside of the first and second regions. Kyker et al. discloses wherein the plurality of regions further includes: a third region corresponding to the sequence number of the data item falling within a sequence number range outside of the first and second regions (Fig. 1, Fig. 3, element 34 (in-order rear-end) is associated with the third region. See col 1, lines 38-47). At the time the invention was made it would have been obvious to a person of ordinary skill in

the art to modify the system of Rana et al. by using the features as taught by Kyker et al. for a more efficient technique to recover from a mispredicted branch in order to reduce the front end stall time (see col 3, lines 43-45).

Regarding Claim 9, Rana et al. discloses a queue engine for reassembling and reordering data packets in a network. Rana et al. does not disclose wherein when the reorder engine classifies the data item as belonging to the first region, the reorder engine stores the information relating to the data item in the reorder buffer. Kyker et al. discloses wherein when the reorder engine classifies the data item as belonging to the first region, the reorder engine stores the information relating to the data item in the reorder buffer (Fig. 4A, element 70, col 4, line 37-48. Note: The reorder buffer (ROB) is in the first region). At the time the invention was made it would have been obvious to a person of ordinary skill in the art to modify the system of Rana et al. by using the features as taught by Kyker et al. for a more efficient technique to recover from a mispredicted branch in order to reduce the front end stall time (see col 3, lines 43-45).

Regarding Claim 10, Rana et al. discloses a queue engine for reassembling and reordering data packets in a network. Rana et al. does not disclose wherein when the reorder engine classifies the data item as belonging to the third region, the reorder engine drops the data item. Kyker et al. discloses wherein when the reorder engine classifies the data item as belonging to the third

region, the reorder engine drops the data item (Fig. 1 and Fig. 3, element 34 (in-order rear end), The Retirement stages 24 are known as the in-order rear end section 34 which is associated with the third region. The entries in this region are retired and deleted in order. See col 1, lines 44-47, col 2, lines 22-33). At the time the invention was made it would have been obvious to a person of ordinary skill in the art to modify the system of Rana et al. by using the features as taught by Kyker et al. for a more efficient technique to recover from a mispredicted branch in order to reduce the front end stall time (see col 3, lines 43-45).

Regarding Claim 11, Rana et al. discloses a queue engine for reassembling and reordering data packets in a network. Rana et al. does not disclose wherein the reorder buffer includes, for each entry in the reorder buffer: a flush bit that stores information indicating whether the external memory contains memory allocated to a previously invalidated entry in the reorder buffer. Kyker et al. discloses wherein the reorder buffer includes, for each entry in the reorder buffer: a flush bit that stores information indicating whether the external memory contains memory allocated to a previously invalidated entry in the reorder buffer (Fig.3 and Fig. 4A, element 78 (mispredict bit (MP)) is equivalent to a flush bit. See col 2, line 54 through col 3, line 9; col 4, line 37 through col 5, line 45). At the time the invention was made it would have been obvious to a person of ordinary skill in the art to modify the system of Rana et al. by using the features as taught by Kyker et al. for a more efficient technique to recover from a

mispredicted branch in order to reduce the front end stall time (see col 3, lines 43-45).

Regarding Claim 13, Rana et al. discloses a queue engine for reassembling and reordering data packets in a network. Rana et al. does not disclose wherein classifying the data items further includes: classifying the data items as belonging to a first region when the sequence number of the data items fall within a sequence number range encompassed by the reorder buffer, and classifying the data items as belonging to a second region when the sequence number of the data item falls within a sequence number range extending from a head of the reorder buffer to a predetermined range beyond the head of the reorder buffer. Kyker et al. discloses wherein classifying the data items further includes: classifying the data items as belonging to a first region when the sequence number of the data items fall within a sequence number range encompassed by the reorder buffer (Fig. 1, Fig. 3, element 30 (in-order front end) is associated with the first region. See col 2, line 33 through col 3, line 21), and classifying the data items as belonging to a second region when the sequence number of the data item falls within a sequence number range extending from a head of the reorder buffer to a predetermined range beyond the head of the reorder buffer (Fig. 1, Fig. 3, element 32 (out of order middle) is associated with the second region. See col 2, line 33 through col 3, line 21). At the time the invention was made it would have been obvious to a person of ordinary skill in

the art to modify the system of Rana et al. by using the features as taught by Kyker et al. for a more efficient technique to recover from a mispredicted branch in order to reduce the front end stall time (see col 3, lines 43-45).

Regarding Claim 14, Rana et al. discloses a queue engine for reassembling and reordering data packets in a network. Rana et al. does not disclose wherein classifying the data items further includes: classifying the data items as belonging to a third region when the sequence number of the data items falls within a sequence number range outside of the first and second regions. Kyker et al. discloses wherein classifying the data items further includes: classifying the data items as belonging to a third region when the sequence number of the data items falls within a sequence number range outside of the first and second regions (Fig. 1, Fig. 3, element 34 (in-order rear-end) is associated with the third region. See col 1, lines 38-47). At the time the invention was made it would have been obvious to a person of ordinary skill in the art to modify the system of Rana et al. by using the features as taught by Kyker et al. for a more efficient technique to recover from a mispredicted branch in order to reduce the front end stall time (see col 3, lines 43-45).

Regarding Claim 16, Rana et al. discloses a queue engine for reassembling and reordering data packets in a network. Rana et al. does not disclose wherein processing the data items includes, when the data items are

classified as belonging to the first region: entering information relating to the data items in the reorder buffer. Kyker et al. discloses wherein processing the data items includes, when the data items are classified as belonging to the first region: entering information relating to the data items in the reorder buffer (Fig. 4A, element 70, col 4, line 37-48. Note: The reorder buffer (ROB) is in the first region). At the time the invention was made it would have been obvious to a person of ordinary skill in the art to modify the system of Rana et al. by using the features as taught by Kyker et al. for a more efficient technique to recover from a mispredicted branch in order to reduce the front end stall time (see col 3, lines 43-45).

Regarding Claim 17, Rana et al. discloses a queue engine for reassembling and reordering data packets in a network. Rana et al. does not disclose wherein processing the data items includes, when the data items are classified as belonging to the third region: dropping the data item. Kyker et al. discloses wherein processing the data items includes, when the data items are classified as belonging to the third region: dropping the data item (Fig. 1 and Fig. 3, element 34 (in-order rear end), The Retirement stages 24 are known as the in-order rear end section 34 which is associated with the third region. The entries in this region are retired and deleted in order. See col 1, lines 44-47, col 2, lines 22-33). At the time the invention was made it would have been obvious to a person of ordinary skill in the art to modify the system of Rana et al. by using the

features as taught by Kyker et al. for a more efficient technique to recover from a mispredicted branch in order to reduce the front end stall time (see col 3, lines 43-45).

7. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Westbrook et al. (U.S. Patent No. 6,832,261) in view of Kyker et al. (U.S. Patent No. 6,026,477).

Regarding Claim 25, Westbrook et al. discloses methods and apparatus for distributed resequencing and distributed reassembly of large packets split into smaller packets with each packet typically marked with a sequence number, timestamp, or other ordering and reassembly indications, and distributed among different paths and arriving possibly out of their original sequence. Westbrook et al. does not disclose wherein the reorder buffer includes, for each entry in the reorder buffer: a flush bit that stores information indicating whether additional processing is required to invalidate the entry in the reorder buffer. Kyker et al. discloses wherein the reorder buffer includes, for each entry in the reorder buffer: a flush bit that stores information indicating whether additional processing is required to invalidate the entry in the reorder buffer (Fig.3 and Fig. 4A, element 78 (mispredict bit (MP)) is equivalent to a flush bit. See col 2, line 54 through col 3, line 9; col 4, line 37 through col 5, line 45). At the time the invention was made it would have been obvious to a person of ordinary skill in the art to use the

mispredict bit or flush bit feature as taught by Kyker et al. in the system of Westbrook et al. for a more efficient technique to recover from a mispredicted branch in order to reduce processing time (see col 3, lines 43-45).

Allowable Subject Matter

8. Claim 8, 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,246,684 to Chapman et al. provides a method and apparatus for re-ordering data traffic units, such as IP data packets, that may have been miss-ordered during a transmission over a multi-pathway link between a source node and a destination node in a network.

U.S. Patent No. 6,862,282 to Oden relates to a method and system for packet ordering in a multi-processor data processing system.

U.S. Patent No. 5,996,067 to White relates to a Range finding circuit for selecting a consecutive sequence of reorder buffer entries using circular carry lookahead.

U.S Publication No. 2003/0039250 to Nichols et al. relates to processing of packet fragments for reassembly into packets and once the fragments are recreated, they are, if required, resequenced using a two-tier memory mapping structure where only pointers, and not the fragments, are manipulated.

U.S Publication No. 2003/0012200 to Salamat provides a method and system for receiving and resequencing out-of-order data packets that permits the use of reduced memory architectures within a router.

The above prior art are cited to further show the same field of endeavor with respect to the applicant's claimed invention.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to F. Lin Khoo whose telephone number is 571-272-5508. The examiner can normally be reached on flex time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WELLINGTON CHIN
SUPERVISORY PATENT EXAMINER